REMARKS

This Amendment responds to the Office Action dated February 2, 2005 in which the Examiner rejected claims 1-3 under 35 U.S.C. §103.

The specification has been amended to correct typographical errors. The Amendment is supported by page 10, line 20. Applicants respectfully request the Examiner approves the correction.

Claim 1 claims a semiconductor integrated circuit comprising a temperature detection circuit including a signal output circuit, a delay circuit, a logic circuit, a pulse width measurement circuit and a latch circuit. The signal output circuit outputs a first signal having at least one rising or falling portion. The delay circuit is formed of at least one inverter to output a delayed version of the first signal. The logic circuit receives the first signal and the delayed version of the first signal. The pulse width measurement circuit outputs a signal asserted in response to a signal received from the logic circuit having a pulse with a width of no less than a predetermined width corresponding to a temperature desired to be detected. The latch circuit latches a signal output from the pulse width measurement circuit. The pulse width measurement circuit has an integration circuit receiving a signal output from the logic circuit and a Schmitt trigger circuit receiving a signal output from the integration circuit. The Schmitt trigger circuit has a trigger potential set to have a value corresponding to the predetermined width.

Through the structure of the claimed invention a) having a pulse width measurement circuit receiving a signal from a logic circuit and b) having a Schmidt trigger circuit of the pulse width measurement circuit receive a signal from an integration circuit as claimed in claim 1, the claimed invention provides a

semiconductor integrated circuit that can have a simple configuration in order to detect temperature. The prior art does not show, teach or suggest the invention as claimed in claim 1.

Claims 1-3 were rejected under 35 U.S.C. §103 as being unpatentable over *Ebihara et al* (U.S. Patent No. 4,237,420) in view of *Nishigaki* (JP 7-326714).

Applicants respectfully traverse the Examiner's rejection of the claims under 35 U.S.C. §103. The claims have been reviewed in light of the Office Action, and for reasons which will be set forth below, applicants respectfully request the Examiner withdraws the rejection to the claims and allows the claims to issue.

Ebihara et al appears to disclose a circuit for measuring temperature changes by means of an monostable multivibrator having a time constant element such as a resistor or capacitor which has a linear response to temperature variations. (col. 1, lines 4-8) FIG. 1 is a circuit diagram of such a conventional type of temperature sensing circuit. Numeral 10 indicates a temperature sensor circuit utilizing an OSM as a temperature sensor. The OSM consists of a two-input NOR gate 12, the output of which is connected to one terminal of a capacitor 16. One end of an adjustable resistor 14 is connected to one side of a power source, designated as Vdd, while the other terminal of resistor 14 is connected to the other terminal of capacitor 16 and to the input terminal of an inverter 18. The output of inverter 18 is connected back to one input of NOR gate 12, and to one input terminal of AND gate 24 of a pulse width measurement circuit 23. The other input terminal of two-input AND gate 24 is connected to a source of clock pulses Cx. (col. 2, lines 7-22) FIG. 2 is a circuit diagram of an embodiment of a temperature sensing circuit. Numeral 11 indicates a temperature sensor circuit utilizing an OSM, which operates in the same manner as

temperature sensor circuit 10 in FIG. 1, but incorporates a three-input NOR gate 32, instead of the two-input NOR gate 12 of the circuit of FIG. 1. Numeral 33 indicates a pulse addition circuit, which is used to add together two successive pulses produced by temperature sensor circuit 11 in a manner to be described later. Pulse addition circuit 33 contains a counter circuit 34, the clock input terminal of which is connected to the output of temperature sensor circuit 11. The output of temperature sensor circuit 11 is also applied to the clock terminal (i.e. the trigger terminal) of an OSM 36. The Q output of OSM 36 is applied to the trigger terminal of another OSM 38, the Q output of which is connected to one input terminal of an AND gate 40. The Q output of OSM 36 is connected to one input terminal of an AND gate 46 in pulse width measurement circuit 44. Output Q2 of counter circuit 34 is connected to the reset terminal of a data type flip-flop 42, the clock terminal of which receives start signal a from start signal source 22. The Q output of data-type flip-flop 42 is connected to the remaining input of AND gate 40, and to one of the input terminals of three-input AND gate 46 of pulse width measurement circuit 44. (col. 3, lines 6-32)

Thus, *Ebihara et al* merely discloses a temperature sensor 11 having an inverter 18 which outputs to a pulse addition circuit 33. Nothing in *Ebihara et al* shows, teaches or suggests a pulse width measurement circuit receiving a signal from a logic circuit as claimed in claim 1. Rather, the inverter 18 of the temperature sensor is output to the pulse addition circuit 33 and not to pulse width measurement circuit 44.

Furthermore, *Ebihara et al* merely discloses a pulse width measurement circuit 44 having an AND gate 46 and a counter circuit 26 and which receives an output from the pulse addition circuit 33 including an output from counter circuit 34.

Nothing in *Ebihara et al* shows, teaches or suggests a pulse width measurement circuit having a Schmitt trigger circuit as claimed in claim 1. Rather, *Ebihara et al* merely discloses a pulse width measurement circuit 44 having a AND gate 46 and a counter circuit 26.

Nishigaki appears to disclose a device for measuring a chip's internal temperature including a buffer circuit 50 and a delay is utilized to measure the chip's internal temperature.

Thus, nothing in *Nishigaki* shows, teaches or suggests a pulse width measurement circuit receiving a signal from a logic circuit and having a Schmitt trigger circuit receive a signal output from an integration circuit as claimed in claim 1.

Since neither *Ebihara et al* nor *Nishigaki* shows, teaches or suggests the structure as claimed in claim 1, applicants respectfully request the Examiner withdraws the rejection to claim 1 under 35 U.S.C. §103.

Claims 2-3 depend from claim 1 and recite additional features. Applicants respectfully submit that claims 2-3 would not have been obvious within the meaning of 35 U.S.C. §103 over *Ebihara et al* and *Nishigaki* at least for the reasons as set forth above. Therefore, applicants respectfully request the Examiner withdraws the rejection to claims 2-3 under 35 U.S.C. §103.

The prior art of record, which is not relied upon, is acknowledged. The references taken singularly or in combination do not anticipate or make obvious the claimed invention.

Thus it now appears that the application is in condition for reconsideration and allowance. Reconsideration and allowance at an early date are respectfully requested.

If for any reason the Examiner feels that the application is not now in condition for allowance, the Examiner is respectfully requested to contact, by telephone, the applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed within the currently set shortened statutory period, applicants respectfully petition for an appropriate extension of time. The fees for such extension of time may be charged to our Deposit Account No. 02-4800.

In the event that any additional fees are due with this paper, please charge our Deposit Account No. 02-4800.

Respectfully submitted,

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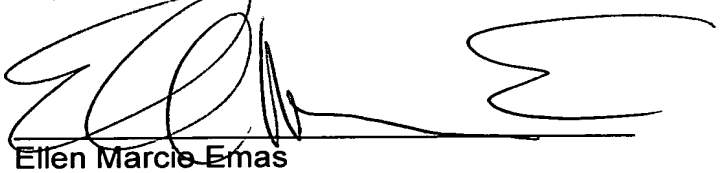
By: 

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